AMENDMENT TO THE CLAIMS

This listing of the claims will replace all prior versions, and listings, of claims in the application.

What is claimed is:

1. (Currently Amended) A semiconductor integrated circuit device comprising:

a terminal; [[and]]

a first capacitance adjusting section which is connected to a wiring between said terminal and a protection resistor in a front stage of an internal circuit; and

a protection circuit which is connected to said wiring between said terminal and said first capacitance adjusting section and protects said internal circuit,

wherein said first capacitance adjusting section adjusts terminal capacitance of said terminal, based on capacitance of said first capacitance adjusting section.

2. (Canceled)

3. (Currently Amended) A [[The]] semiconductor integrated circuit device ~~according to Claim 1,~~ comprising:

a terminal; and

a first capacitance adjusting section which is connected to a wiring between said terminal and a protection resistor in a front stage of an internal circuit,

wherein said first capacitance adjusting section adjusts terminal capacitance of said terminal, based on capacitance of said first capacitance adjusting section,

wherein said first capacitance adjusting section comprises a first adjusting capacitor which adjusts said terminal capacitance, and

wherein said first adjusting capacitor comprises:

a first semiconductive portion which is composed of a first well region formed in a substrate with said internal circuit and having a conductive type opposite to that of said substrate, and

a second semiconductive portion which is opposite to said first semiconductive portion and is composed of a first diffusion layer region formed in said first well region and having the same conductive type as that of said substrate.

4. (Original) A [[The]] semiconductor integrated circuit device ~~according to Claim 3,~~ comprising:

a terminal;

a first capacitance adjusting section which is connected to a wiring between said terminal and a protection resistor in front stage of an internal circuit, and

a well potential control section,

wherein said first capacitance adjusting section adjusts terminal capacitance of said terminal, based on capacitance of said first capacitance adjusting section,

wherein said first capacitance adjusting section comprises a first adjusting capacitor which adjusts said terminal capacitance,

wherein said first adjusting capacitor comprises:

a first semiconductive portion which is composed of a first well region formed in a substrate with said internal circuit and having a conductive type opposite to that of said substrate, and

a second semiconductive portion which is opposite to said first semiconductive portion and is composed of a first diffusion layer region formed in said first well region and having the same conductive type as that of said substrate,

wherein said first capacitance adjusting section further comprises a second adjusting capacitor which adjusts said terminal capacitance based on controlling a well region potential by said well potential control section,

wherein said second adjusting capacitor comprises:

a third semiconductive portion which is composed of a second well region formed in said substrate and having a conductive type opposite to that of said substrate,

a fourth semiconductive portion which is opposite to said third semiconductive portion and is composed of a second diffusion layer region formed in said second well region and having the same conductive type as that of said substrate, and

wherein said well potential control section controls said well region potential of said second well region.

5. (Original) The semiconductor integrated circuit device according to Claim 4, wherein said well potential control section comprises:

a plurality of resistors which are connected in series to each other between two potential electrodes; and

a plurality of switches each of which is connected in parallel to each of said plurality of resistors,

said well potential control section controls said well region potential by controlling each one of said plurality of switches.

6. (Original) The semiconductor integrated circuit device according to Claim 5, further comprising:

a plurality of said terminals; and

a plurality of said first capacitance adjusting sections, each of which is connected to said wiring between each of said plurality of terminals and each of a plurality of said protection resistors,

wherein said well potential control section controls each of a plurality of said well region potentials.

7. (Currently Amended) The semiconductor integrated circuit device according to Claim [[2]] 1, wherein said first capacitance adjusting section comprises a first adjusting capacitor which adjusts said terminal capacitance,

said first adjusting capacitor comprises:

a first semiconductive portion which is composed of a first well region formed in a substrate with said internal circuit and having a conductive type opposite to that of said substrate, and

a second semiconductive portion which is opposite to said first semiconductive portion and is composed of a first diffusion layer region formed in said first well region and having the same conductive type as that of said substrate.

8. (Original) The semiconductor integrated circuit device according to Claim 7, further comprising:

a well potential control section,

wherein said first capacitance adjusting section further comprises a second adjusting capacitor which adjusts said terminal capacitance based on controlling a well region potential by said well potential control section,

said second adjusting capacitor comprises:

a third semiconductive portion which is composed of a second well region formed in said substrate and having a conductive type opposite to that of said substrate,

a fourth semiconductive portion which is opposite to said third semiconductive portion and is composed of a second diffusion layer region formed in said second well region and having the same conductive type as that of said substrate, and

said well potential control section controls said well region potential of said second well region.

9. (Original) The semiconductor integrated circuit device according to Claim 8, wherein said well potential control section comprises:

a plurality of resistors which are connected in series to each other between two potential electrodes; and

a plurality of switches each of which is connected in parallel to each of said plurality of resistors,

said well potential control section controls said well region potential by controlling each one of said plurality of switches.

10. (Original) The semiconductor integrated circuit device according to Claim 9, further comprising:

a plurality of said terminals; and

a plurality of said first capacitance adjusting sections each of which is connected to each of a plurality of said wirings between each of said plurality of terminals and each of a plurality of said protection resistors,

wherein said well potential control section controls each of a plurality of said well region potentials.

11. (Original) The semiconductor integrated circuit device according to Claim 1, further comprising:

a second capacitance adjusting section which is connected to a wiring between said first capacitance adjusting section and said internal circuit, wherein said second capacitance adjusting section adjusts said terminal capacitance based on capacitance of said second capacitance adjusting section; and

a switching control section which controls said capacitance of said second capacitance adjusting section.

12. (Original) The semiconductor integrated circuit device according to Claim 11, wherein said switching control section comprises:

a plurality of switches each of which outputs signal potentials corresponding to turn on and off of said each of plurality of switches, and

a plurality of signal holding sections each of which holds corresponding each of a plurality of said signal potentials,

wherein said switching control section controls said capacitance of said second capacitance adjusting section based on said plurality of signal potentials.

13. (Original) The semiconductor integrated circuit device according to Claim 12, wherein said second capacitance adjusting section comprises:

a plurality of third adjusting capacitors each of which capacitance is variable based on corresponding said each of said plurality of signal potentials,

wherein said second capacitance adjusting section adjusts said plurality of third adjusting capacitors based on said plurality of signal potentials.

14. (Original) The semiconductor integrated circuit device according to Claim 13, further comprising:

a plurality of said terminals; and

a plurality of said second capacitance adjusting sections each of which is connected to each of a plurality of said wirings between each of said plurality of said first capacitance adjusting sections and each of a plurality of said internal circuits,

wherein said switching control section controls each of a plurality of said capacitances of said plurality of second capacitance adjusting sections.

15. (Original) The semiconductor integrated circuit device according to Claim 3, further comprising:

a second capacitance adjusting section which is connected to a wiring between said first capacitance adjusting section and said internal circuit, wherein said second capacitance adjusting section adjusts said terminal capacitance based on capacitance of said second capacitance adjusting section; and

a switching control section which controls said capacitance of said second capacitance adjusting section.

16. (Original) The semiconductor integrated circuit device according to Claim 15, wherein said switching control section comprises:

a plurality of switches each of which outputs signal potentials corresponding to turn on and off of said each of plurality of switches, and

a plurality of signal holding sections each of which holds corresponding each of a plurality of said signal potentials,

wherein said switching control section controls said capacitance of said second capacitance adjusting section based on said plurality of signal potentials.

17. (Original) The semiconductor integrated circuit device according to Claim 16, wherein said second capacitance adjusting section comprises:

a plurality of third adjusting capacitors each of which capacitance is variable based on corresponding said each of said plurality of signal potentials,

wherein said second capacitance adjusting section adjusts said plurality of third adjusting capacitors based on said signal potential.

18. (Original) The semiconductor integrated circuit device according to Claim 17, further comprising:

a plurality of said terminals; and

a plurality of said second capacitance adjusting sections each of which is connected to each of a plurality of said wirings between each of said plurality of said first capacitance adjusting sections and each of a plurality of said internal circuits ,

wherein said switching control section controls each of a plurality of said capacitances of said plurality of second capacitance adjusting sections.